

Micromachined Thermal Radiation Emitter from a Commercial CMOS Process

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Abstract—Fabrication of thermally isolated micromechanical structures capable of generating thermal radiation for dynamic thermal scene simulation (DTSS) is described. Complete compatibility with a commercial CMOS process is achieved through design of a novel, but acceptable, layout for implementation by the CMOS foundry using its regular process sequence. Following commercial production and delivery of the CMOS chips, a single maskless etch in an aqueous ethylenediamine-pyrocatechol mixture (EDP) is performed to realize the micromechanical structures. The resulting structures are suspended plates consisting of polysilicon resistors encapsulated in the field and CVD oxides available in the CMOS process. The plates are suspended by aluminum heater leads that are also encapsulated in the field and CVD oxides. Studies of the suitability of these structures for DTSS have been initiated, and early favorable results are reported.

I. INTRODUCTION

TWO-DIMENSIONAL arrays of miniature thermal radiation emitters and associated control circuits are needed for dynamic thermal scene simulation (DTSS) [1]. For applications requiring large arrays, each emitter must be integrated with its own addressable control circuit in order that the finished devices have a practical pin or lead count. Silicon micromachining technology based on IC-compatible processes and materials has already been used to produce thermal and visible radiation sources on chips [2]–[5]. The recent successful use of a commercial CMOS process for fabricating micromechanical structures [6], [7] suggests that it might be possible to integrate arrays of emitters and their associated control circuits on a single chip using a commercial CMOS process. Indeed, the heater structure originally developed for use as a gas flow sensor described in [7] would seem to satisfy the requirements of DTSS [1]. Our letter reports the results of testing this and similar CMOS micromachined heater structures for suitability in DTSS.

II. DEVICE FABRICATION AND YIELD

Fabrication of the micromechanical heater structure for use as a thermal radiation source is similar to the technique reported in [6] and [7]. For the chip designer, it involves nothing more than submitting a special layout design to the CMOS foundry, and carrying out a single maskless etch after receiving finished CMOS chips from the foundry.

Our designs were fabricated by Northern Telecom Canada

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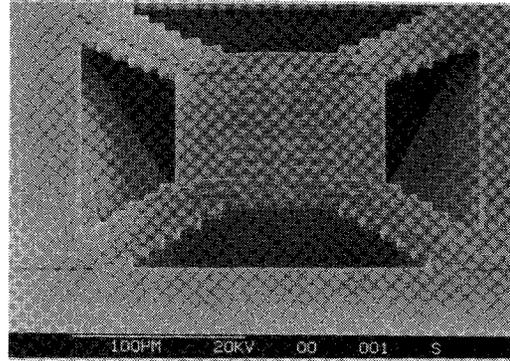


Fig. 1. SEM photograph of the thermally isolated CMOS heater structure showing the polysilicon resistor elements and the aluminum leads encapsulated in the field and CVD oxides.

Ltd. using their COMS3 DLM (3 μm , 13 mask) process. The important features of the design are the definition of the active area, contact cut, and pad opening layers of the CMOS layout in order to expose selected areas of the silicon substrate [6]. The resistors used as heater elements are defined in the polysilicon layer of the CMOS process, and are encapsulated in the field and CVD oxides. The heater leads, which serve to suspend the heater elements, are defined in the metal layer, and are also encapsulated in the field and CVD oxide layers. This type of design, upon implementation in the CMOS process, provides an IC chip that contains the basic structures for forming the micromechanical heater structures. The maskless etch in an ethylenediamine-pyrocatechol mixture (EDP) anisotropically etches the substrate silicon and forms a cavity for thermal isolation of the heater structure only at the sites where the silicon has been exposed in accord with the layout design [7]. An SEM photograph of one of the heater structures is shown in Fig. 1. The resistor heater elements formed from the polysilicon and the aluminum heater leads can be clearly seen in the photograph.

To date, 80 chips (20 each from four submissions) having heater structures similar or identical to that shown in Fig. 1 have been fabricated. The resistances of all of the heater elements on all of the chips were measured and found to be consistent with the foundry-specified standard deviation of 20% of the design value. The first attempt at etching included four chips. None of the heater structures on these chips was completely freed due to insufficient time in the etching bath. About 66 more chips were etched, with a few from each batch being reserved as unetched controls. Not all of the structures have been tested following etching, but no failures have been discovered among those that have been tested, except when 45 mW or more is dissipated in one of the resistor elements as described below. One batch of chips had both p-type and n-type CMOS FET's as well as heater structures. The characteristics of these FET's did not change

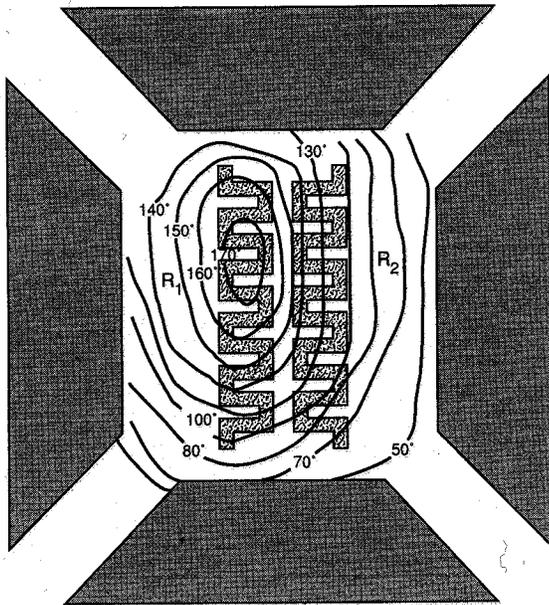


Fig. 2. A spatial map of the temperature distribution of the heater structure shown in Fig. 1 for a current of 3 mA in one resistor element on the left, R_1 .

following exposure to the etching solution during the post-processing etch that freed the heater structures.

There are four very attractive features of this approach to fabricating arrays of heaters on silicon chips for DTSS. Firstly, as is the case for IC circuits designed for production at a foundry, the device designer need not know the processing details of the CMOS technology employed by the foundry. All that is required is the preparation of a suitable layout using a graphics terminal running the appropriate layout software. Secondly, no modifications to the CMOS process sequence are required at any stage. Indeed, it would greatly diminish the usefulness of the approach if any modifications were required. Thirdly, the post-processing etch is easily implemented since it requires no mask. Lastly, the post-processing etch does not affect the circuits formed on the chip. Hence, the full power of the circuit-forming capability of the CMOS process remains at the designer's disposal, so that on-chip control electronics can be integrated into the design.

III. SUITABILITY FOR DYNAMIC THERMAL SCENE SIMULATION

To confirm the applicability to DTSS of the results reported in [7], which were obtained from electro-thermal response measurements, the spatial temperature distribution over one of the micromachined heater structures was measured using an infrared (IR) microscope. The measured temperature distribution for a steady-state current of 3 mA through resistor element R_1 is sketched in Fig. 2. From the data in that figure, the average temperature of the resistor element R_2 was calculated to be 130°C. Considering the uncertainties associated with the various measurements and the coarse grid of the temperature distribution in Fig. 2, this value is in surprisingly close agreement with the value of 128°C reported for an identical element in [7].

To be useful for DTSS, the micromechanical heater structure shown in Fig. 1 must be capable of cycling over its useful temperature range a great number of times without failure, and its resistance should remain within some reasonable range during its lifetime. In some applications of DTSS, 300°C is a useful

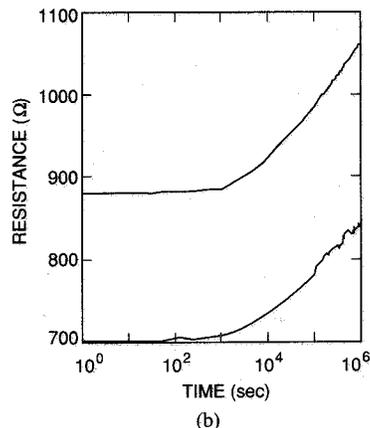
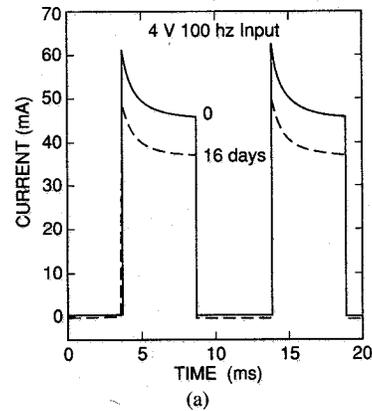


Fig. 3. Comparison (a) of the current response of one of the resistor elements shown in Fig. 1 to a 4-V, 100-Hz square wave at the start of the lifetime testing and 16 days later, and (b) of the resistance of the resistor element at the beginning of the 4-V pulse (lower curve), and at the end of the 4-V pulse (upper curve).

upper temperature limit. To test the suitability of the structure of Fig. 1 for these applications, one of the resistors was excited continuously for a number of weeks by a 4-V, 100-Hz, 50% duty-cycle square wave. Fig. 3(a) compares the current waveform during two cycles at the beginning of the test and two cycles 16 days later. These waveforms show the change in heater resistance with temperature during the 4-V pulse; the resistor element nearly reaches its steady-state temperature just before the applied voltage is switched off.

Fig. 3(b) plots the resistance near room temperature and the resistance at the highest temperature reached during each cycle as a function of time for 10^8 temperature cycles. At the start of the test, the resistor element is dissipating 18.3 mW at the end of each voltage pulse, corresponding to an element temperature of approximately 334°C. After 10^8 cycles, the test resistor is dissipating 15.1 mW at the end of each pulse, corresponding to a temperature of 280°C. This test is continuing toward 10^9 cycles, and the element resistance is still behaving as shown in Fig. 3(b).

Also, as part of the reliability testing, the power dissipated in one of the structures identical to that shown in Fig. 1 was increased until the polysilicon resistor element failed. During these tests the current-carrying resistor, as observed under an optical microscope, became incandescent. It started to emit a mild red glow near the center of the resistor element at about 30 mW (4.9 mA), and was glowing very brightly over more than 70% of its length at about 45 mW (6.3 mA), at which point it quickly failed.

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