

Micromachined Microwave Transmission Lines in CMOS Technology

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Abstract—Coplanar waveguides were designed and fabricated through a commercial CMOS process with post-processing micromachining. The transmission-line layouts were designed with commercial computer-aided design (CAD) tools. Integrated circuits (IC's) were fabricated through the MOSIS service, and subsequently suspended by top-side etching. The absence of the lossy silicon substrate after etching results in significantly improved insertion-loss characteristics, dispersion characteristics, and phase velocity. Two types of layout are presented for different ranges of characteristic impedance. Measurements of the waveguides both before and after micromachining were performed at frequencies from 1 to 40 GHz using a vector network analyzer and de-embedding techniques, showing improvement of loss characteristics of orders of magnitude. For the entire range of frequencies, for the 50- Ω layout, losses do not exceed 4 dB/cm. These losses are mainly due to the small width and thickness of the metal strips. Before etching, losses are as high as 38 dB/cm due to currents in the underlying substrate. Phase velocity in the micromachined transmission lines is close to that in free space.

Index Terms— CMOS microwave elements, coplanar waveguides, maskless etching, micromachining, MOSIS, suspended transmission lines.

I. INTRODUCTION

WITH constantly increasing frequencies in communications and integrated circuits, there is a great demand for low-cost, miniature microwave components [1]–[3]. In many applications, there is also a need for easy integration with analog and digital circuits [4], [5]. The planarization of transmission lines to microstrip, stripline, and coplanar-waveguide has provided much flexibility in design, reduced weight and volume, and cost of production. Planar components have reduced in size so much that their fabrication by conventional machining techniques has become too costly and difficult. It is for this reason that the recent advances in micromachining techniques have been finding numerous applications in the microwave field. Various passive microwave components fabricated by micromachining have been proposed by others [1]–[5], showing the numerous advantages of such

designs. However, in previous work, many photolithographical masking steps, both on the top and bottom side of the wafer, are needed for micromachining and metal deposition [1]–[3]. The processes also include wafer bonding and are not compatible with commercially available computer-aided design (CAD) tools and CMOS foundries. Consequently, they do not provide easy integration with analog and digital circuits.

This paper presents the design of miniature microwave transmission lines through a standard CMOS process with subsequent top-side etching. The transmission lines were designed in a commercial CAD tool, as part of a standard CMOS design, and fabricated through the MOSIS service [6]. As part of the CAD layout, regions of superimposed glass cuts, called *open* areas [7], were included. Due to such design, the CMOS-fabricated chips already included areas of exposed silicon substrate for etching, requiring no additional masks. This is described in detail in Section II-B. The removal of the silicon substrate material in the vicinity of the metal structures significantly improves the insertion-loss characteristics, frequency-response bandwidth, transmission-line dispersion characteristics, phase velocity, and impedance-control capability.

The described process of obtaining microwave transmission lines on silicon substrates is comparably simple and low-cost. Also, fabricating the microwave components through commercial CMOS foundries gives the capability for monolithic integration with standard CMOS circuits. In the future, these advantages may allow larger scale integration in sensor, communications, and other applications. The advantages, however, are tradeoffs with slightly lesser performance because the conductive films available in the CMOS fabrication process (first- and second-layer aluminum) are not optimal for the design.

In the following sections, the authors present the design of the coplanar waveguides, the post-CMOS fabrication process steps, and the results of electrical performance tests.

II. DESIGN AND FABRICATION

A. Design of Coplanar Waveguides

The transmission lines were designed to operate in TEM mode, with 50- and 120- Ω nominal characteristic impedance. Two different characteristic impedances were designed to test two different kinds of layouts which require a slightly different etching procedure and are applicable for different ranges of desired characteristic impedance. Simplified diagrams of the

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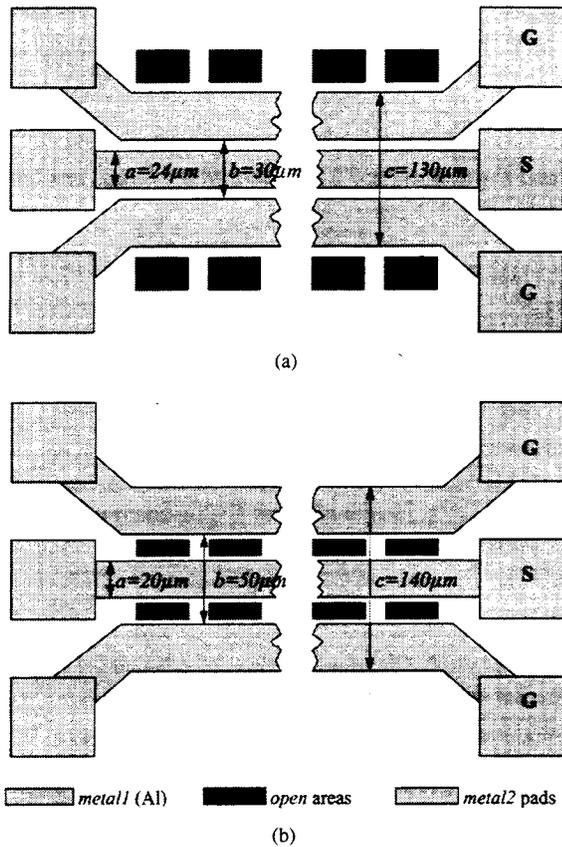


Fig. 1. Simplified layouts of the coplanar waveguides for CMOS implementation. (a) *Open areas* (glass cuts) outside the ground planes. (b) *Open areas* between signal and ground planes.

layouts are shown in Fig. 1, showing the three coplanar waveguide strips in ground-signal-ground (GSG) configuration, the electrical probing pads, and the *open areas* which are necessary for micromachining of fabricated integrated circuits (IC's). Cross-sectional diagrams of the structures in Fig. 2 show the important waveguide dimensions which determine the characteristic impedance and propagation modes. It can be seen in Fig. 1(a) and (b) that the only difference in the layouts is the placement of the *open areas* which expose the substrate for post-fabrication etching.

Characteristic impedance of coplanar waveguides in terms of the line dimensions can be approximated from conformal mapping methods by the following:

$$Z_0 = \frac{\eta_0}{4.0 \cdot \sqrt{\epsilon_{\text{eff}}}} \cdot \frac{K(k)}{K(k')} \quad (1)$$

where η_0 is the free-space impedance, ϵ_{eff} is the effective dielectric constant of the medium, k and k' parameters are defined by line dimensions

$$k = \frac{c}{b} \sqrt{\frac{b^2 - a^2}{c^2 - a^2}}, \quad k' = \sqrt{1 - k^2} \quad (2)$$

and $K(k)/K(k')$ is the ratio of first-order elliptic integrals of the first kind [8]. In standard CMOS processes, metal layers are fully encapsulated in glass, as shown in Fig. 2, which makes it difficult to accurately estimate the effective dielectric constant

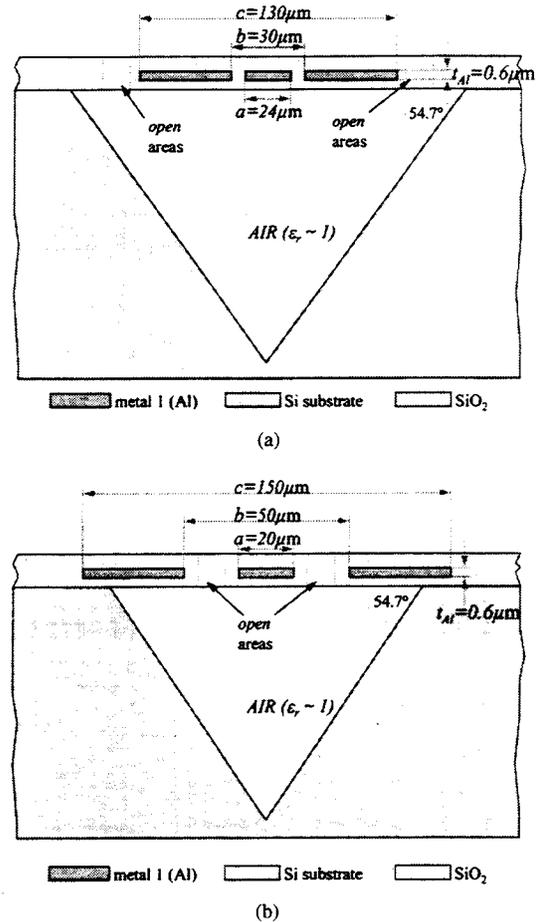


Fig. 2. Cross-sectional diagram of the transmission-line structures with the etched V-shaped pit. (a) *Open areas* outside the ground planes. (b) *Open areas* between signal and ground planes.

ϵ_{eff} . From quasi-static finite-element simulations, $\epsilon_{\text{eff}} = 2.18$ is obtained for the $50\text{-}\Omega$ structure in Fig. 2(a), and $\epsilon_{\text{eff}} = 1.45$ for the $120\text{-}\Omega$ structure in Fig. 2(b). These values have proved to be good approximations in agreement with the best values extracted from measurements as shown in Section IV.

B. CMOS Implementation and Etching Procedure

The layout for the transmission lines was created in Magic [7], a public-domain CAD graphics layout editor. The conductor strips were laid out in the first-layer metal (aluminum). The waveguides connect with electrical probing pads in GSG configuration, with $160\text{-}\mu\text{m}$ pitch. The pads consist of both first- and second-layer metal connected by many vias.

To fabricate the micromachined transmission-line elements, one must design a structure that incorporates appropriate openings in the glass layers. Glass cuts must be patterned in such a way as to allow the chemical etch to produce the desired cavity under the metal strips and also provide mechanical support for the structure. The openings in the glass layers are designed using the *open layer* [7] in Magic, which incorporates all of the necessary glass cuts to expose the silicon substrate. The corresponding Caltech intermediate form (CIF) layers are active area—“CAA,” active contact—“CCA,” via—“CVA,”

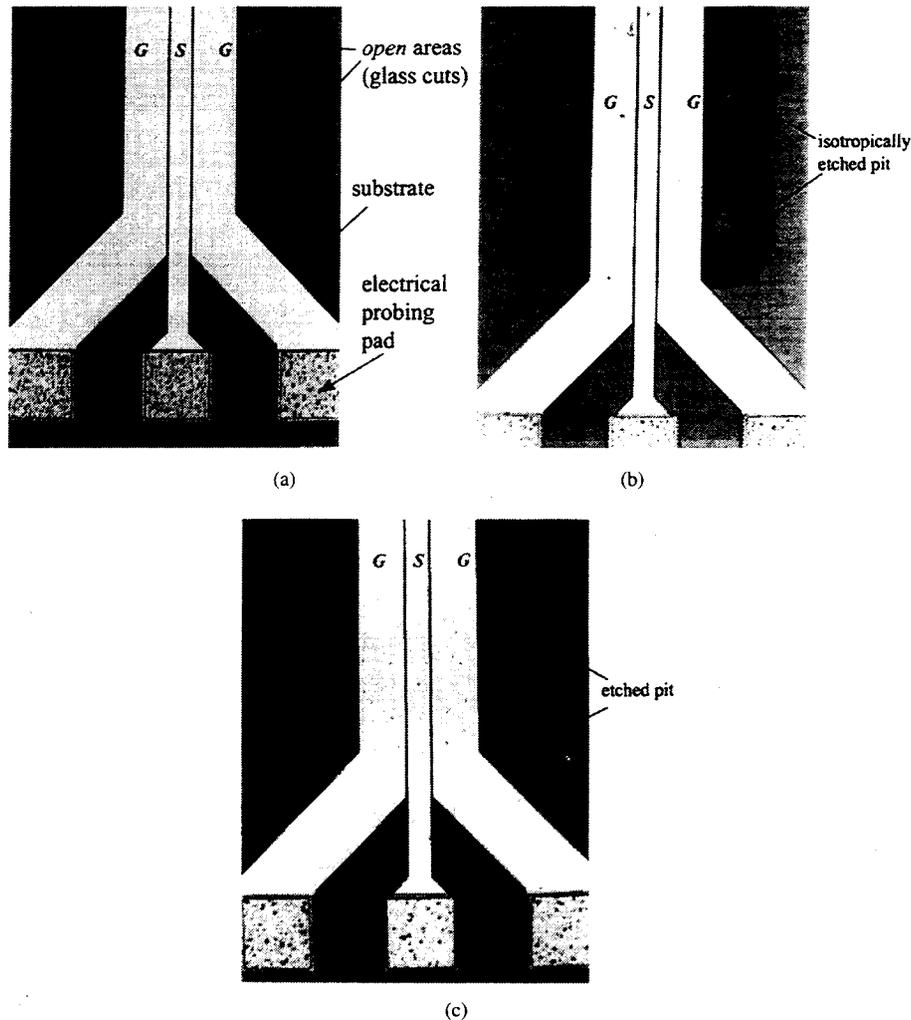


Fig. 3. Microphotograph of the 50- Ω coplanar waveguide (a) after CMOS fabrication, (b) after isotropic etch, and (c) after combined etch.

and overglass opening—"COG." This subsequently permits the etchant to penetrate from the top side of the chip and remove the substrate material from beneath the transmission lines, leaving only the desired metal and the encapsulating glass. As illustrated in Fig. 1, the *open* areas were designed on both sides of the metal strips, with enough spacing between them to ensure that the structure would remain mechanically stable after micromachining. In the layout for the higher characteristic impedance, the glass cuts are placed on both sides of the signal strip, between the signal and ground planes, as shown in Fig. 1(b). Such a layout results in a somewhat smaller etch pit as illustrated in Fig. 2(b), and, therefore, requires less etching time and allows for closer integration of the waveguide structures. When lower characteristic impedance is needed, the *open* areas are placed outside the ground planes as shown in Fig. 1(a). The metal strips can then be spaced much closer, down to the minimum design rule spacing for first-layer metal.

The IC's are fabricated in a commercial 2- μm CMOS n-well process, on a 460- μm -thick $\langle 100 \rangle$ wafer. The fabricated structures already include appropriately placed glass cuts, as mentioned earlier, and are ready for etching. A section of

the 50- Ω coplanar waveguide with electrical probing pads is shown in the microphotograph in Fig. 3(a). The photograph shows the three aluminum strips and rectangular glass cuts on both sides of the waveguide. The chips are etched in two steps. In the first step, a gaseous isotropic etchant, xenon difluoride (XeF_2) [9], is applied. Isotropic etch creates small cavities around each *open* area which propagate outwards radially. After approximately 16 min of etching (32 30-s pulses), the cavities from the two sides of the waveguides connect beneath the signal line. At that point, in the second step, the chips are etched by an anisotropic etchant, ethylene diamine-pyrocatechol water (EDP) [7]. The anisotropic etch follows the crystalline structure of the $\langle 100 \rangle$ wafer, forming a V-shaped pit as shown in Fig. 2. The completed walls of the etched pit slope at an angle of 54.7° from the surface plane and are aligned to the $\langle 111 \rangle$ crystallographic plane of the substrate material. In effect, an inverted pyramid-shaped trough is formed by the micromachining step. The EDP etch takes approximately 1 h at 92°C . It is important to continue etching until the trough is fully formed to secure good electromagnetic isolation of the transmission line from the substrate. The fabricated transmission lines are shown in Fig. 3(a) and (b).

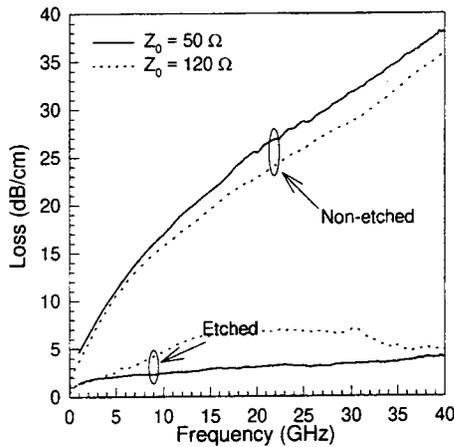
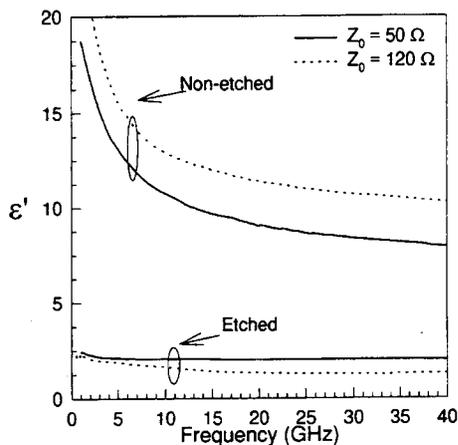
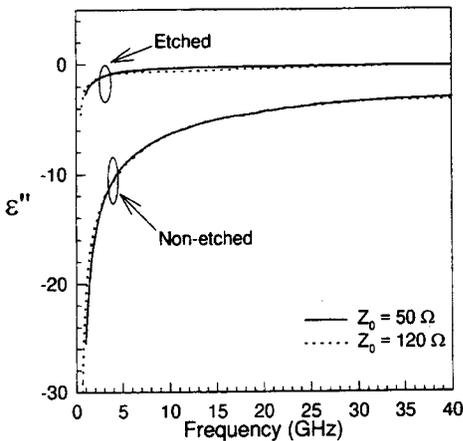


Fig. 4. Attenuation measurements of the transmission lines before and after etching.



(a)



(b)

Fig. 5. Measured effective dielectric constant of the transmission lines before and after etching. (a) Real part. (b) Imaginary part.

III. MEASUREMENT SETUP

For the experimental characterization of the transmission behavior of the transmission lines, the test chip included

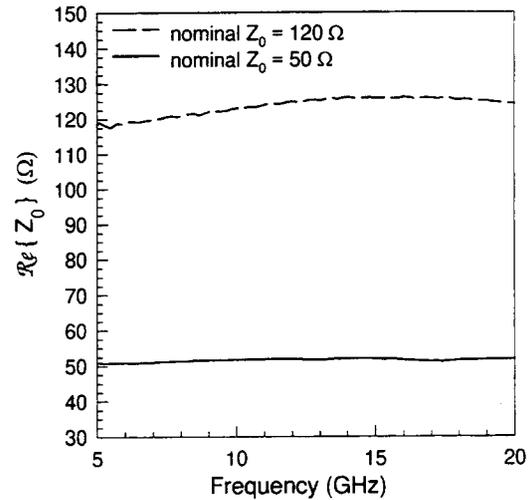


Fig. 6. Measured real part of characteristic impedance for etched lines.

lines of three different lengths along with short and open stubs. The longest line was 3.7-mm long, while the thru was 0.8 mm. Measurements were performed at frequencies in the 1–40-GHz range, using the HP8510B¹ automatic network analyzer and a microwave probing station. A full set of measurements was performed on the transmission-line elements both before and after micromachining. In both cases, one-tier thru-reflect-line (TRL) [10] calibration was performed on three lines of different lengths, and short and open stubs. Because the sizes of the structures were small compared to the wavelengths of the test signals, the parasitic effects caused by the probes and contact pads had to be carefully characterized in order to minimize their influence on the measurements. The probe placement had to be performed with high precision in order to ensure accurate phase measurements. From the de-embedded measurements [11], [12] of the *s*-parameters, the propagation constant per-unit length and the effective dielectric constant was extracted at each frequency.

Insertion loss was calculated from transmission-line measurements before and after etching. The attenuation results in Fig. 4 are given in dB/cm length. The measurements of the effective complex dielectric constant, $\epsilon_{\text{eff}} = \epsilon' + j \cdot \epsilon''$ are shown in Fig. 5(a) and (b).

From the measured complex propagation constant, the characteristic impedances of the etched transmission lines was computed using the method described in [12] after measuring the capacitance per-unit length [13]. Results for the 5–20 GHz range are shown in Fig. 6.

IV. DISCUSSION OF THE RESULTS

The measurements of transmission-line insertion loss and effective dielectric constant show great improvement in performance after the structures were suspended. The results

¹Certain commercial products are identified in this paper to specify the procedure adequately. This does not imply recommendation or endorsement by NIST, nor does it imply that those commercial products are the best available for the purpose.

are very similar for both layouts. At 20 GHz, insertion loss is decreased 24 dB, while at 40 GHz, a 34-dB improvement is shown. The micromachined 50- Ω waveguides exhibit lower attenuation as expected due to wider metal strips.

Absence of the lossy silicon substrate ($\epsilon_{Si} = 11.7$) gives much better dispersion characteristics and higher phase velocity. Recently, methods for increasing phase velocity in coplanar waveguides have been proposed [3], [14] outlining the need for extremely fast transmission lines. The authors' proposed methodology could possibly find similar applications. The micromachined transmission lines have phase velocity slightly below that in free space $v_p \approx 0.9 \cdot c$. Before etching, at 20 GHz, $v_p \approx c/3$, while at 1 GHz, the phase velocity is even lower due to the slow-wave mode of propagation [15] $v_p \approx c/5$. From the real part of dielectric constant shown in Fig. 5(a), it can be seen that the 120- Ω lines have slightly lower ϵ' , and, therefore, slightly higher v_p . This was expected since the layout for these lines includes glass cuts between the signal and ground planes, with most of the electric field energy concentrated in air and only a portion in glass.

Unfortunately, the overall performance of the new transmission lines is limited by the relatively high series impedance in the metal strips due to the very small thickness of the metal layers in CMOS. Because this is not an available MOSIS design parameter, the thickness cannot be varied, and losses can be further decreased only by increasing the linewidths.

V. CONCLUSIONS AND FUTURE WORK

A new design for transmission lines suitable for application to a broad class of sensors and integrated circuits was described. The authors have proposed applications of this methodology for implementation of low-cost microwave power sensors on CMOS chips [16], [17]. The new transmission line is electrically, thermally, and mechanically isolated from the surrounding medium by a process of micromachining of the semiconductor substrate material in the vicinity of the transmission line. The advantages of the proposed design are the low cost of fabrication and monolithic integration with analog and digital CMOS circuits. The availability of microwave structures on CMOS substrates might, in the future, allow for larger-scale integration for sensor and communication circuits at greatly lowered costs. Although the proposed structures were fabricated in a commercial CMOS process, the concept is applicable to both silicon integrated-circuit technology and gallium arsenide (GaAs) microwave integrated-circuit technology.

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